WHAT IS CLAIMED IS:

1. A method for forming a semiconductor device, comprising:

etching a first portion of a dielectric layer with a first etch chemistry; and

etching a second portion of the dielectric layer with a second etch chemistry different from the first etch chemistry.

2. The method of claim 1, wherein the dielectric layer is substantially continuous.

3. The method of claim 1, wherein an interface does not exist between the first and second portions of the dielectric layer.

4. The method of claim 1, wherein a thickness of the first portion of the dielectric layer is greater than a thickness of the second portion of the dielectric layer.

5. The method of claim 1, wherein a thickness of the second portion of the dielectric layer is greater than approximately one half of a height of an adjacent gate structure.

6. The method of claim 1, wherein the first etch chemistry is substantially free of hydrogen.

7. The method of claim 1, wherein the first etch chemistry comprises C_4F_8 and CO.

8. The method of claim 1, wherein the second etch chemistry comprises at least one hydrogen-containing compound.

9. The method of claim 1, wherein the second etch chemistry comprises $C_2H_2F_4$.

10. The method of claim 1, wherein the second etch chemistry comprises CHF_3.

11. The method of claim 1, further comprising forming said dielectric layer in one processing step.

12. The method of claim 1, wherein the first etch chemistry has a dielectric layer material:silicon nitride selectivity of at least approximately 10:1.

13. The method of claim 1, wherein the second etch chemistry has a dielectric layer material:silicon oxide selectivity of at least approximately 5:1.

14. The method of claim 1, wherein the dielectric layer comprises a doped silicon oxide having a phosphorus concentration of less than approximately 6 wt. %.

15. The method of claim 1, wherein the dielectric layer is in contact with a sidewall spacer of a gate structure and a semiconductor layer comprising isolation regions.

16. The method of claim 15, wherein etching the first portion of the dielectric layer exposes an upper corner of the sidewall spacer, and wherein etching the second portion of the dielectric layer exposes the semiconductor layer.

17. A method for forming a contact hole, comprising:

depositing a dielectric layer upon first and second gate laterally spaced gate structures on a semiconductor layer comprising isolation regions;

etching a first portion of the dielectric layer with a first etch chemistry; and

etching a second portion of the dielectric layer with a second etch chemistry, wherein a thickness of the second portion of the dielectric layer is greater than approximately one half of a height of the first and second gate structures.

18. The method of claim 17, wherein the first etch chemistry is selective to silicon nitride, and wherein the second etch chemistry is selective to silicon dioxide.

19. The method of claim 16, wherein the dielectric layer comprises a doped silicon oxide having a phosphorus concentration of less than approximately 6 wt.%.

20. The method of claim 16, wherein etching the first portion of the dielectric layer exposes upper corners of the first and second gate structures, and wherein etching the second portion of the dielectric layer exposes the semiconductor layer.

21. A method for forming a self aligned contact hole, comprising:

etching a first portion of a substantially continuous dielectric layer adjacent to a gate structure with a first etch chemistry substantially free of hydrogen sufficiently to expose a sidewall spacer of said gate structure; and

etching a second portion of the substantially continuous dielectric layer with a second etch chemistry comprising a hydrofluorocarbon etchant sufficiently to expose a substrate under said substantially continuous dielectric layer.